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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,117	05/30/2006	Jozef Pieter Van Gassel	NL 031406	5189

24737 7590 07/22/2008

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
SNYDER, STEVEN G	

ART UNIT	PAPER NUMBER
2184	

MAIL DATE	DELIVERY MODE
07/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,117	VAN GASSEL ET AL.	
	Examiner	Art Unit	
	STEVEN G. SNYDER	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is in response to communication filed on March 12, 2008.

Status of Claims

Claims 1 to 20 are pending, of which claims 1, 9, and 13 are in independent form.

Claim Rejections - 35 USC § 112

In light of applicant's amendments to claim 5, the examiner withdraws the rejection to claim 5.

Response to Arguments

The examiner again suggests that applicants amend the specification to include headings as shown in MPEP 608.01(a). Since this is the format that the overwhelming majority of patent applications follow, the specification would then be more easily understood.

1. Applicant's arguments filed March 12, 2008 have been fully considered but they are not persuasive.

Applicant argues in regards to claim 1, "the office action fails to identify where Kever or Korst teaches or suggests determining an optimum buffer size for which the power consumption of a subsystem of a mass storage device and a buffer memory is a

minimum for a given streaming bit-rate to/from said buffer memory" (page 6 lines 24 – 28).

The examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider each of the cited references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage disclosed by the examiner. Therefore, as shown in the rejection below, the examiner believes that all of the above limitations are taught by Kever and Korst.

Applicant argues in regards to claim 9, "The Office action fails to identify where Kever or Korst teaches a processing unit that adaptively activates or deactivates areas of said buffer memory in such a manner that total power consumption of a subsystem comprising a storage device and a buffer memory is minimized for a given streaming rate to/from said buffer memory" (page 6 line 29 – page 7 line 2).

The examiner disagrees. Kever's paragraph [0009], previously cited by the examiner states "The PMU then turns on the appropriate amount of cache memory needed for that application." Also, paragraph [0005] describes the PMU being "on a microprocessor." Further, paragraph [0007] discloses turning off power to memory sections that are not being accessed. As in the previous office action, Korst was cited

to show how the memory of Kever could be connected to a hard disk drive. Further, Korst describes how variable bit-rate schedulers may be used to determine which streams require more data. Therefore, the examiner believes that all of the above limitations are taught or suggested by Kever and Korst, and the rejection below states a motivation to combine Kever and Korst.

Applicant argues, "Neither Kever nor Korst teaches or suggests controlling a buffer size to minimize the power consumption of a subsystem of a mass storage device and buffer memory, and the Office action fails to identify where either Kever or Korst provides this teaching" (page 7 lines 6 – 9) and "the cited text of Kever fails to address minimizing the power consumption of a subsystem of a mass storage device and buffer memory. Kever merely teaches controlling the amount of active memory based on the amount of memory needed by an application, which will not necessarily minimize the amount of energy used by the memory, nor minimize the amount of energy used by a storage device, and specifically will not necessarily minimize the amount of energy consumed by the combination of the memory and storage device" (page 7 lines 19 – 25).

The examiner disagrees. Kever was cited in the previous office action to teach turning on and off sections of memory for the purpose of saving power (paragraph [0008]). Therefore, when Korst shows connecting the memory of Kever with a hard disk drive, the total power consumption of both buffer memory and a mass storage device

would inherently be minimized. Also, the rejection below states a motivation to combine Kever and Korst.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1 – 4, 6, 9 – 14, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kever et al., U.S. Patent Application 2003/0145239 (hereinafter referred to as Kever) in view of Korst et al., U.S. Patent 6,061,732 (hereinafter referred to as Korst).**

Referring to claim 1, Kever discloses "a method for adaptively minimising the total power consumption of an apparatus" ([0008], sections of cache memory may be turned on or off depending on the current needs of the system). Kever also discloses "said method comprising the steps of determining an optimum buffer size for which the power consumption of said subsystem is a minimum" and "adjusting the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal ([0009] – [0010], a monitor controls which section of memory

is turned on or off based on signals from a software application indicating how much memory the application needs).

Kever does not appear to explicitly disclose determining an optimum buffer size "for a given streaming bit-rate to/from said buffer memory." Also, Kever does not appear to explicitly disclose the memory sections being connected to a hard disk drive.

However, Korst discloses a scheduling scheme that "determines for which stream data needs to be read" (column 2 lines 21 – 25). Korst further discloses using a variable bit-rate scheduler determining which streams require more data (column 2 lines 58 – 67). Finally, Korst also discloses a hard disk drive connected to a plurality of memory buffers (Fig. 1, storage medium 110 and column 8 lines 16 – 18, "storage unit, such as a hard disk").

Kever and Korst are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever and Korst before him or her, to modify the teachings of Kever to include the teachings of Korst, so that the memory described in Kever would be connected to a hard disk drive and bit-rates would be used to determine when to turn a memory section on or off.

The motivation for doing so would have been to provide a means to handle fixed consumption rate systems as well as variable consumption rate systems, which are both described by Korst (column 2 lines 46 – 67).

Therefore, it would have been obvious to combine Korst with Kever to obtain the invention as specified in the instant claim(s).

As per claim 2, Kever discloses "adjusting the buffer size comprises switching on memory banks and/or memory ICs of said buffer memory for increasing the size of said buffer memory, and switching off memory banks and/or memory ICs for decreasing said buffer memory" (Figs. 1 and 2, switches S11 – S13 and S21 – S23 are used to control whether or not each memory array is powered (on) or not powered (off)).

As per claim 3, Kever discloses how an application may indicate how much memory the application needs ([0010]). Kever also discloses how a monitor controls which section of memory is turned on or off based on signals from a software application indicating how much memory the application needs ([0009] – [0010]).

Kever does not appear to explicitly disclose "determining a harddisk drive data rate, determining the stream bit-rate to/from the buffer memory, and determining the optimum buffer size having the lowest power consumption at the determined stream bit-rate."

However, Korst discloses a scheduler being used for load balancing between a rate of reading from the hard disk and a stream bit rate associated with the buffer memory (column 2 lines 21 – 45 and column 5 line 66 – column 6 line 7). Korst also

discloses how a variable bit-rate scheduler determines which streams require more data and which streams have a buffer with room for more data (column 2 lines 58 – 67).

Kever and Korst are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever and Korst before him or her, to modify the teachings of Kever to include the teachings of Korst, so that the memory described in Kever would be connected to a hard disk drive, and bit-rate to/from the buffer memory and the hard disk drive data rate would be used to determine when to turn a memory section on or off for the purposes of saving power.

The motivation for doing so would have been to provide a means to handle fixed consumption rate systems as well as variable consumption rate systems, which are both described by Korst (column 2 lines 46 – 67).

Therefore, it would have been obvious to combine Korst with Kever to obtain the invention as specified in the instant claim(s).

As per claim 4, Kever does not appear to explicitly disclose the "optimum buffer size determination step comprises calculating optimum buffer size from a formula, looking up optimum buffer size in a look-up table, or measuring the minimum power consumption of the subsystem in a feedback loop controlling buffer size."

However, Korst discloses an equation using the data rate of the hard disk along with the data stream bit rate to determine how much memory is necessary (column 4 line 56 – column 5 line 18).

Kever and Korst are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever and Korst before him or her, to modify the teachings of Kever to include the teachings of Korst, so that the determination of how much memory is needed would be based on the result of a formula.

The motivation for doing so would have been to provide a simple means for determining how much memory is needed.

Therefore, it would have been obvious to combine Korst with Kever to obtain the invention as specified in the instant claim(s).

As per claim 6, Kever discloses "powering up extra memory banks and/or memory ICs when a new stream is admitted" ([0008], power can be saved by turning off memory sections that aren't needed and turning on memory sections when other applications require it. Also, [0010], applications may send signals to turn on or off memory sections while the application is running).

Referring to claim 9, claim 1 recites corresponding limitations as that of claim 9. Therefore, the rejection of claim 1 applies to claim 9. Further limitations of claim 9 are discussed below.

Kever discloses the circuit comprising "a processing unit" ([0005], a PMU (performance monitor unit) being "on a microprocessor").

Kever does not appear to explicitly disclose a step to "retrieve the data from the mass storage device."

However, Korst discloses a method for reading data stored in a hard disk (Fig. 1).

Kever and Korst are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever and Korst before him or her, to modify the teachings of Kever to include the teachings of Korst, so that the memory described in Kever would be connected to a hard disk drive and data could be read from the hard disk.

The motivation for doing so would have been to include a more permanent and larger memory device in the apparatus.

Therefore, it would have been obvious to combine Korst with Kever to obtain the invention as specified in the instant claim(s).

As per claim 10, Kever does not appear to explicitly disclose a system including a hard disk drive and buffer memory.

However, Korst discloses a system including a hard disk drive and buffer memory (Fig. 1).

Kever and Korst are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever and Korst before him or her, to modify the teachings of Kever to include the teachings of Korst, so that the memory described in Kever would be connected to a hard disk drive and both the buffer memory and hard disk drive would be held in a single apparatus.

The motivation for doing so would have been to include an apparatus that could handle fixed and variable consumption rate streams, as described by Korst.

Therefore, it would have been obvious to combine Korst with Kever to obtain the invention as specified in the instant claim(s).

As per claim 11, Kever discloses independently switching memory banks on and off (Fig. 1).

Kever does not appear to explicitly disclose those memory banks being SDRAM circuits.

However, Korst discloses how buffer memory comprises SDRAM circuits having banks of memory adapted to be independently switched on/off (column 9 lines 65 – 66, the buffers are usually implemented using RAM).

Kever and Korst are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever and Korst before him or her, to modify the teachings of Kever to include the teachings of Korst, so that the memory described in Kever would be implemented using RAM.

The suggestion for doing so can be seen in Korst's disclosure (column 9 lines 65 – 66).

Therefore, it would have been obvious to combine Korst with Kever to obtain the invention as specified in the instant claim(s).

As per claim 12, Kever does not appear to explicitly disclose "a scheduler function executable by the processing unit controls accessing the storage device and the buffer memory."

However, Korst discloses a scheduler 170 that is incorporated in the system and controls the transfer of data between the hard disk and the buffer memory (Fig. 1).

Kever and Korst are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever and Korst before him or her, to modify the teachings of Kever to include the teachings of Korst, so that a scheduler controls access to the storage device and buffer memory.

The suggestion for doing so can be seen in Korst's disclosure (column 2 lines 21 – 25), which describes the scheduler ensuring efficient use of buffers.

Therefore, it would have been obvious to combine Korst with Kever to obtain the invention as specified in the instant claim(s).

Referring to claim 13, Kever discloses "a computer-readable medium having embodied thereon a computer program for processing by a computer, the computer program comprising code segments for adaptively minimising the total power consumption of a subsystem" and a "code segment adjusts the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal" ([0010], an application sends signals to instruct the switching on or off of memory sections. Also, [0005], a microprocessor being used to monitor the system and switch memory sections on or off).

Furthermore, it is known in the art that microprocessors carry out actions based on code segments.

Kever does not appear to explicitly disclose a subsystem "comprising a mass storage device and a buffer memory." Kever also does not disclose a "code segment

determines an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate from said buffer memory."

However, Korst discloses a system including a mass storage device (Fig. 1). Korst also achieves the aspect of determining an optimum buffer size based on a formula (column 4 line 56 – column 5 line 18).

Kever and Korst are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever and Korst before him or her, to modify the teachings of Kever to include the teachings of Korst, so that the buffer memory is connected to a hard drive and the application uses an equation to determine an optimum buffer size.

The motivation for doing so would have been to use the processor's capabilities to run the equation in order to determine which memory sections should be turned on or off.

Therefore, it would have been obvious to combine Korst with Kever to obtain the invention as specified in the instant claim(s).

Note, claim 14 recites the corresponding limitations of claim 3. Therefore, the rejection of claim 3 applies to claim 14.

Note, claim 20 recites the corresponding limitations of claim 12. Therefore, the rejection of claim 12 applies to claim 20.

3. **Claims 5 and 15 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kever in view of Korst, as applied to claims 1 – 4, 6, and 9 – 13 above, and further in view of Kling et al., U.S. Patent Application 2001/0003207 (hereinafter referred to as Kling).**

As per claim 5, Kever discloses memory sections that can be turned on or off (Fig. 1).

Also, Korst discloses a scheduler being used for load balancing between a rate of reading from the hard disk and a stream bit rate associated with the buffer memory (column 2 lines 21 – 45 and column 5 line 66 – column 6 line 7).

Neither Kever nor Korst appears to explicitly disclose using a "ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption."

However, Kling discloses monitoring power consumption by measuring the duty cycle ([0018]).

Kever, Korst, and Kling are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever, Korst, and Kling before him or her, to modify the teachings of Kever and Korst to include the teachings of Kling so that duty cycle measurements could be used to monitor power consumption.

The motivation for doing so would have been to provide an alternate means for determining which memory sections should be turned on or off.

Therefore, it would have been obvious to combine Kling with Korst and Kever to obtain the invention as specified in the instant claim(s).

Note, claim 15 recites the corresponding limitations of claim 5. Therefore, the rejection of claim 5 applies to claim 15.

Note, claim 16 recites the corresponding limitations of claim 5. Therefore, the rejection of claim 5 applies to claim 16.

Note, claim 17 recites the corresponding limitations of claim 5. Therefore, the rejection of claim 5 applies to claim 17.

Note, claim 18 recites the corresponding limitations of claim 5. Therefore, the rejection of claim 5 applies to claim 18.

4. **Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kever in view of Korst, as applied to claims 1 – 4, 6, and 9 – 13 above, and further in view of Yoshida, U.S. Patent 5,928,365 (hereinafter referred to as Yoshida).**

As per claim 7, neither Kever nor Korst appears to explicitly disclose moving data stored in a memory section that is to be powered down into a memory that will remain powered.

However, Yoshida discloses saving the contents of a memory section that will be switched off into another memory (column 9 line 53 – column 10 line 10).

Kever, Korst, and Yoshida are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever, Korst, and Yoshida before him or her, to modify the teachings of Kever and Korst to include the teachings of Yoshida so that memory sections that are about to be switched off would have their data moved to a section that will remain on.

The motivation for doing so would have been to provide a means for ensuring that data is not lost when a memory section is turned off.

Therefore, it would have been obvious to combine Yoshida with Korst and Kever to obtain the invention as specified in the instant claim(s).

Note, claim 19 recites the corresponding limitations of claim 7. Therefore, the rejection of claim 7 applies to claim 19.

5. **Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kever in view of Korst, as applied to claims 1 – 4, 6, and 9 – 13 above, and further in view of Falcon, Jr. et al., U.S. Patent 5,712,976 (hereinafter referred to as Falcon, Jr.).**

As per claim 8, neither Kever nor Korst appears to explicitly disclose adding the bit rates of all simultaneous streams to determine an optimum buffer size.

However, Falcon, Jr. discloses ensuring that the size of memory can support the maximum number of simultaneous streams (column 31 line 48 – column 32 line 7).

Kever, Korst, and Falcon, Jr. are analogous art because they are from the same field of endeavor, which is methods of using memories.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Kever, Korst, and Falcon, Jr. before him or her, to modify the teachings of Kever and Korst to include the teachings of Falcon, Jr. so that the system would ensure that the maximum number of simultaneous streams can be supported by the memory.

The motivation for doing so would have been to provide a means for ensuring that data is not lost.

Therefore, it would have been obvious to combine Falcon, Jr. with Korst and Kever to obtain the invention as specified in the instant claim(s).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent **5,898,880** and application **2003/0154246**.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN G. SNYDER whose telephone number is (571)270-1971. The examiner can normally be reached on Mon. - Thurs. 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

S.S.

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181